## CLAIMS

1. A network interface card including:

a system interface circuit arrangement;

a network interface circuit arrangement;

a storage for storing a set of patterns;

a storage for storing mask data identifying patterns to be matched; and

a pattern match logic circuit arrangement correlating marked patterns with other data and generating at least one first control signal if a match occurs between one of the marked patterns and the other data.

2. The network interface card of claim 1 further including a host computer coupled to the system interface, said host computer including software for downloading to the network interface card the set of patterns and the mask data.

3. The network interface card of claims 1 or 2 further including address match function logic circuit for correlating an address for the network interface card and a received address and generating a second control signal on the occurrence of a match.

4. The network interface card of claims 1 or 2 wherein each pattern in the set of patterns are arranged in 4 (four) bytes wide words and 128 byte sectors.

5. The network interface card of claim 4 wherein the patterns are arranged contiguously in the Mask Storage.

6. The network interface card of claim 4 wherein the mask data is arranged so that each M-bits word of mask contains mask bits for words in N patterns, where M=number of bits in a word and N=number of patterns.

7. The network interface card of claim 4 wherein M = 32 and N = 8.

8. The network interface card of claim 1 wherein the pattern match logic circuit arrangement includes a first state machine for assembling data received from the network interface circuit arrangement into predetermined sizes and identifying beginnings and endings of data frames; and

a second state machine coupled to the first state machine, said second state including means for receiving the predetermined sizes from the first state machine and means for generating addresses for accessing the pattern storage and mask storage, whereat data are to be read and used with the predetermined sizes in generating the ~~first control signal.~~

9. The network interface card of claim 8 wherein the address generation ~~means~~ circuit uses the expression YYYxxxxx to determine the addresses for the Pattern RAM, wherein xxxxx represents an index count and YYY represents states for a state machine.

10. The network interface card of claim 1 wherein the system interface circuit arrangement includes a PCI Interface.

11. The network interface of claim 1 wherein the network interface circuit arrangement includes Ethernet MII Interface.

12. A pattern matching method including the steps of:

(a) providing a set of patterns;

(b) providing a set of data;

(c) providing mask for identifying portions of the patterns;

(d) correlating data, from the set of data, with identified portions in step (c); and

(e) generating a Match signal if the data of step (d) and the identified portion of the pattern match.

13. A method for using in a communications network to wake station connected to the communications network said method including the steps of:

(a) providing, on a network interface card, a set of patterns against which data from the communications network is to be matched;

(b) providing mask data indicating portions of a pattern to be used;

(c) correlating each identified portion with data received from the communications network; and

(d) generating a Wake-Up signal if a match occurs in step (c).

14. The method of claim 13 further including the steps of (e) correlating a station address with an address received with the data from the communications network; and

(f) generating the Wake-Up signal only if a match occurs (step e) and a ~~match occurs (step e),~~

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